

Claims

- [c1] 1.A state saving circuit comprising:
a first latch capable of performing a desired operation,
the first latch being powered by a first power supply; and
a second latch capable of restoring the state of the first
latch upon the powering up of the first latch.
- [c2] 2.The state saving circuit of claim 1,
wherein said power supply comprises an un-interruptible
power supply and
further comprising a cut-off control device powered by
the un-interruptible power supply that selectively con-
nects the second latch to a pair of latch nodes based
upon a control signal, wherein the control signal deter-
mines whether said second latch is in one of a state sav-
ing mode and a state restoring mode.
- [c3] 3.A state saving circuit comprising:
a state saving latch powered by an un-interruptible
power supply; and
a cut-off control device powered by the un-interruptible
power supply that selectively connects the state saving
latch to a pair of latch nodes based upon a control sig-
nal, wherein the control signal determines whether said

state-saving latch is in one of a state saving mode and a state restoring mode.

- [c4] 4.The state saving circuit of claim 3 wherein said state saving latch comprises a pair of cross coupled inverters.
- [c5] 5.The state saving circuit of claim 4, wherein the pair of cross coupled inverters comprise a pair of CMOS inverters.
- [c6] 6.The state saving circuit of claim 5, wherein the pair of CMOS inverters comprise high threshold voltage devices.
- [c7] 7.The state saving circuit of claim 3, wherein said cut-off control device disconnects the state saving latch from the pair of latch nodes when the control signal has a predetermined low value.
- [c8] 8.The state saving circuit of claim 3, wherein said cut-off control device comprises a CMOS inverter.
- [c9] 9.The state saving circuit of claim 8, wherein said CMOS inverter comprises a high threshold voltage device.
- [c10] 10.The state saving circuit of claim 8, wherein said cut-off control device further comprises a pair of transistors each having a gate in communication with an output of the CMOS inverter.

- [c11] 11.The state saving circuit of claim 3, wherein said state saving latch comprises a CMOS inverter.
- [c12] 12.The state saving circuit of claim 3, wherein the latch nodes comprise a true latch node and a complement latch node.
- [c13] 13.The state saving circuit of claim 3, wherein the cut-off control device comprises:
an inverter receiving said control signal, that inverts said control signal and provides said inverted control signal to gates of a first pair of transistors; and
a second pair of transistors receiving said control signal at the gates of said second pair of transistors.
- [c14] 14.The state saving circuit of claim 13, wherein said latch nodes comprise a true node and a complement node.
- [c15] 15.The state saving circuit of claim 14, wherein one of said first pair of transistors is connected to said true node and the other of said first pair of transistors is connected to said complement node.
- [c16] 16.The state saving circuit of claim 13, wherein said state saving latch comprises a pair of cross coupled inverters.

- [c17] 17.The state saving circuit of claim 16, further comprising a third pair of transistors selectively connecting said first pair of transistors to a ground based upon input gate signals from said pair of cross-coupled inverters.
- [c18] 18.The state saving circuit of claim 16, further comprising a third pair of transistors selectively connecting said second pair of transistors to a ground based upon input gate signals from a said pair of cross-coupled inverters.
- [c19] 19.A circuit, comprising:
a D flip flop powered by an interruptible power supply and comprising a pair of latch nodes;
a state saving latch powered by an un-interruptible power supply; and
a cut-off control device powered by the un-interruptible power supply that selectively connects the state saving latch to said pair of latch nodes based upon a control signal,
wherein the control signal determines whether said state-saving latch is in one of a state saving mode for enabling said state saving latch to follow a state of said D flip flop and a state restoring mode for restoring the state of said D flip flop from said state saving latch.
- [c20] 20.A circuit, comprising:
an application specific integrated circuit powered by an

interruptible power supply and comprising a pair of latch nodes;

a state saving latch powered by an un-interruptible power supply; and

a cut-off control device powered by the un-interruptible power supply that selectively connects the state saving latch to said pair of latch nodes based upon a control signal,

wherein the control signal determines whether said state-saving latch is in one of a state saving mode for enabling said state saving latch to follow a state of said application specific integrated circuit and a state restoring mode for restoring the state of said application specific integrated circuit from said state saving latch.